Category	IP Name	Description
Data Integrity	aip_128b130b_encoder	This iP is used to encode data at data rate 8.0GT/s or higher. PCI Express 3.0 uses a different encoding system, called 128b/130b. 128b/130b encoding is a Link-wide packetization mechanism and a per-Lane block code with scrambling. As you can deduce, this encoding system transmits each 128 bits of data as a 130-bit number, which offers a far lower overhead. To transmit 128 bits of data, PCI Express 3.0 needs only two extra bits, while with the previous revisions, 32 extra bits are needed (two for every eight bits).
Data Integrity	aip_128b130b_scrambler	The scrambling logic for 128b/130b is modified from the previous PCIe generations to address the two issues that 8b/10b encoding handled automatically: maintaining DC Balance and providing a sufficient transition density. By way of review, recall that DC Balance means the bit stream has an equal number of ones and zeros.
Data Integrity	aip_128b130b_decoder	This IP is used to decode data 128b/130b from encoding system 128b130b Encoder
Data Integrity	aip_128b130b_descrambler	Receivers follow exactly the same rules for generating the scrambling polynomial that the Transmitter does and simply XOR the same value to the input data a second time to recover the original information. Like on the transmit side, they are allowed to implement a separate LFSR for each Lane or just one.
Data Integrity	aip_8b10b_encoder	This IP is a line code that maps 8-bit words to 10-bit symbols to achieve DC-balance and bounded disparity, and yet provide enough state changes to allow reasonable clock recovery. This means that the difference between the counts of ones and zeros in a string of at least 20 bits is no more than two, and that there are not more than five ones or zeros in a row. This helps to reduce the demand for the lower bandwidth limit of the channel necessary to transfer the signal
Data Integrity	aip_8b10b_decoder	provides 10-bit to 9-bit decoding, includes 8-bit data and 1-bit data control. The parallel 10-bit binary input represent 1024 values, called symbols, but only 464 symbols are valid (decoding to 256 data values, and 12 special symbols)
Data Integrity	aip_8b10b_scrambler	The Scrambler eliminates generation of repetitive patterns on a transmitted data stream. Example, when scrambled, a stream of 0s will result in a pseudo-random bit pattern.
Data Integrity	aip_binenc	Binary Encoder
Data Integrity	aip_decode	Binary Decoder
Data Integrity	aip_decode_en	Binary Decoder with Enable
Data Integrity	aip_crc	CRC data generator for DDR protocol
Data Integrity	aip_crc_gen	CRC generator (LCRC or ECRC)
Data Integrity	aip_dllp_crc	DLLP LCRC generator
Data Integrity	aip_ecc	Error Checking and Correction
Data Integrity	aip_ecrc	Calculation of ECRC for TLP-Packets of PCIe Protocol
Data Integrity	aip_first_one_detect	First bit '1' detector
Data Integrity	aip_first_zero_detect	First bit '0' detector
Data Integrity	aip_last_zero_detect	Last bit '0' detector
Data Integrity	aip_lcrc	Calculation of LCRC for DLLP-Packets of PCIe Protocol
Data Integrity	aip_par_gen	Parity Generator and Checker (ODD or EVEN parity)
Data Integrity	aip_parity	Even Parity Generator
Data Integrity	aip_prbs_gen	Tx Pattern Generator. Sequence generator for testing signal integrity of high-speed link, ncludes Pseudo-random bit sequences, square wave and PCI Express compliance pattern generators
Data Integrity	aip_prbs_ver	Rx Pattern Checker. Check one of five industry-standard PRBS pattern: PRBS-7, PRBS-9, PRBS-15, PRBS-23 and PRBS-21
Data Integrity	aip_pricod	Priority Encoder
Control Logic	aip_arb_fcfs	First-Come-First-Served Arbiter
Control Logic	aip_arbiter_2t	Two-Tier Arbiter
Control Logic	aip_arb_pri_mask	Arbiter Priority Mask
Control Logic	aip_arb_rr	Round-Robin Arbiter
Logic Component	aip_bicnt_dwn	Down Binary Counter with Count-to and Step-count
Logic Component	aip_bictr_dcnto	Up/Down Binary Counter with Dynamic Count-to Flag
Logic Component	aip_bictr_dcnto_up	Up Binary Counter with Dynamic Count-to Flag
Logic Component	aip_bictr_rcnto_up	Up Binary Counter with Dynamic Count-to Flag (Turn around)
Logic Component	aip_block_alignment	Block alignment for 128b130b encoding
Logic Component	aip_command_priority_filter	Command priority filter
Logic Component	aip_dwncnt	Down Binary Counter with Count-to and Count-Clear

Logic Component	aip_lfsr_dcnto	LFSR Counter with Dynamic Count-to Flag
Logic Component	aip_lfsr_dcnto_up	Wrapper for LFSR Counter with Dynamic Count_to Flag
Logic Component	aip_lfsr_load	LFSR Counter with Loadable Input
Logic Component	aip_lfsr_rcnto_reload_up	Wrapper for LFSR Counter with Registered Count_to Flag
Logic Component	aip_lfsr_rcnto_up	LFSR Counter with Registered Count_to Flag
Logic Component	aip_malloc_ctl	Asynchronous Allocation Module with Dynamic Burst-length (Combine with Reordering Buffer)
Logic Component	aip_mux_any	Universal Multiplexer
Logic Component	aip_mux_any_onehot	The universal multiplexer with one-hot selector
Logic Component	aip_mux_onehot	The universal multiplexer with one-hot selector and default value
Logic Component	aip_one_counter_onehot	Bit '1' counter with onehot output
Logic Component	aip_pipe_reg	Pipeline register
Logic Component	aip_pl_reg	Pipeline Register - with individual enable
Logic Component	aip_rd_dbi	Read Data Bus Inversion
Logic Component	aip_read_resp_buf_ctl	Read response reordering buffer with allocation
Logic Component	aip_reg_s_pl	Register with Synchronous Enable Reset
Logic Component	aip_row_shft	The universal variable-offset (distance) row shifter
Logic Component	aip_shad_reg	Shadow and Multibit Register
Logic Component	aip_shftreg	Shift Register with parallel output
Logic Component	aip_shift_reg	Shift Register with parallel and serial output
Logic Component	aip_shiftreg_piso	Shift Register Parallel Input Serial Output
Logic Component	aip_wr_dbi	Write Data Bus Inversion
FIFO	aip_asymdata_inbuf	Asymmetric Data Input Buffer
FIFO	aip_asymdata_outbuf	Asymmetric Data Output Buffer
FIFO	aip_fifo_async_sf	Asynchronous First-In-First-Out buffer with static status flag
FIFO	aip_fifo_s1_df	Synchronous (single clock) FIFO with Dynamic Flags
FIFO	aip_fifo_s1_sf	Synchronous (single clock) FIFO with Static Flags
FIFO	aip_fifo_s1_sf_r	Synchronous (single clock) FIFO with static flags and output register
FIFO	aip_ram_r_w_s_dff	Sync. Write Port – Async. Read Port RAM (Flip-Flop-Based)
FIFO	aip_xq	Crossover Queue
FIFO Controller	aip_asymfifoctl_s1_df	Asymmetric I/O Synch. (One Clock) FIFO Controller, with Dynamic Flags
FIFO Controller	aip_fifoctl_s1_df	Synchronous (single clock) FIFO Controller with Dynamic Flags
FIFO Controller	aip_reorder_buf_ctl_s1	Synchronous (single clock domain) Reordering Buffer Controller
FIFO Controller	aip_write_data_buf_ctl	Write data reordering buffer with allocation
Arithmetic Component	aip_brent_kung_adder	Use to add two numbers base on the Brent Kung algorithm. Optimize for area
Arithmetic Component	aip_kogge_stone_adder	Use to add two numbers base on the Kogge Stone algorithm. Optimize for speed
Arithmetic Component	aip_bin_to_gray	Binary to Gray code converter
Arithmetic Component	aip_gearbox	Convert the input data words into a different word size
Arithmetic Component	aip_compressor662	Compressor 66 to 2 bit
Arithmetic Component	aip_divider	A Sequential Divider
Arithmetic Component	aip_gray_to_bin	Gray to Binary code converter
Arithmetic Component	aip_booth_wallace	Use to multiply two numbers base on the Booth Wallace algorithm. Optimize for speed
Arithmetic Component	aip_vedic_addad	Use to multiply two numbers base on the Vedic and Addad algorithm. Optimize for area
Arithmetic Component	aip_fp_adder	Floating point adder
Arithmetic Component	aip_fp_mult	Floating point multiply
Arithmetic Component	aip_fp_mac	Floating point MAC
Arithmetic Component	aip_pipe_fp_adder	Floating point adder pipeline
Arithmetic Component	aip_pipe_fp_mult	Floating point multiply pipeline
Arithmetic Component	aip_pipe_fp_mac	Floating point MAC pipeline
Arithmetic Component	aip_onehot_to_binary	Onehot to Binary code converter
Interface	aip_cdc_data_sync	Clock Domain Crossing Data Synchronize
Interface	aip_tap_controller	JTAG Controller
Interface	aip_uart	UART/USART Controller
Interface	aip_spi	Serial Peripheral Interface Controller
Interface	aip_qspi	Quad-Serial Peripheral Interface Controller
Interface	aip_ospi	Octal- Serial Peripheral Interface Controller
Interface	aip_ssi	Synchronous Serial Interface Controller
Interface	aip_i2c	I2C (Inter-Integrated Circuit) Interface Controller
Interface	aip_i2s	Inter-IC Sound Bus Controller
Interface	aip_i3c	I3C Interface Controller
Interface	aip_gpio	General-purpose Input/Output Controller
Interface	aip_pwm	Pulse Width Modulator Controller
Interface	aip_ictrl	Interrupt Controller

Interface	aip_spi_to_i2c	Convert SPI to I2C interface
Interface	aip_spi_to_uart	Convert SPI to UART interface
Memory IPs	aip_memory	aip_memory DDR2/DDR3/DDR4/LPDDR2/LPDDR3/LPDDR4 multichannel external memory controller
Memory IPs	aip_emmc	aip_emmc controller
Memory IPs	aip_sd	aip_sd host controller. It supports both legacy and ultra-high speed II (UHS-II) interfaces.
Memory IPs	testpiler	A memory BIST solution which has been optimized for AIP memories
Verification IP	aip_apb_vip	APB verification IP
Verification IP	aip_axi4_bfm	AXI4 Master Bus-Functional-Model
Verification IP	aip_axi4lite_bfm	AXI4-Lite Master Bus-Functional-Model
Verification IP	aip_axi4lite_vip	AXI4-Lite Verification IP
Verification IP	aip_axi4_vip	AXI4 Verification IP
Verification IP	aip_common	Common Functions for Verification
Verification IP	aip_pcie_vip	PCIe Verification IP
Verification IP	aip_sequence_manage	Sequence manager
Verification IP	aip_sysclk_ctrl	System Clock Generator
Timer	aip_wdt	Watchdog Timer
Timer	aip_rtc	Real-time Clock
Other IP	aip_pvt_monitor	Monitor delay in different PVT conditions
Other IP	aip_temperature_monitor	Monitor temperature sensor

Category	IP Name	Description
Interface	aip_tap_controller	JTAG Controller
Interface	aip_uart	UART/USART Controller
Interface	aip_spi	Serial Peripheral Interface Controller
Interface	aip_qspi	Quad-Serial Peripheral Interface Controller
Interface	aip_ospi	Octal- Serial Peripheral Interface Controller
Interface	aip_ssi	Synchronous Serial Interface Controller
Interface	aip_i2c	I2C (Inter-Integrated Circuit) Interface Controller
Interface	aip_i2s	Inter-IC Sound Bus Controller
Interface	aip_i3c	I3C Interface Controller
Interface	aip_gpio	General-purpose Input/Output Controller
Interface	aip_pwm	Pulse Width Modulator Controller
Interface	aip_ictrl	Interrupt Controller
Interface	aip_spi_to_i2c	Convert SPI to I2C interface
Interface	aip_spi_to_uart	Convert SPI to UART interface
Memory IPs	aip_memory	aip_memory DDR2/DDR3/DDR4/LPDDR2/LPDDR3/LPDDR4 multichannel external memory controller
Memory IPs	aip_emmc	aip_emmc controller
Memory IPs	aip_sd	aip_sd host controller. It supports both legacy and ultra-high speed II (UHS-II) interfaces.
Timer	aip_wdt	Watchdog Timer
Timer	aip_rtc	Real-time Clock